

1. A circuit to drive a high-voltage H-bridge using CMOS technology comprising:

a control logic circuit having an input and an output, wherein the input comprises control signals defining the behavior of said H-bridge and the output are control signals for the high-side and low-side drivers of said H-bridge;

5 a power management module having an input and an output wherein the input is a battery voltage and the output is a voltage to feed the low-side drivers and means to drive at the battery voltage level;

a means to drive at the battery voltage level to drive the high-side drivers of the H-bridge and a means for reverse supply protection;

10 a means for reverse supply protection;

two high-side drivers having an input and an output, wherein the input are control signals from said control logic circuit and a voltage from said charge pump and the output is driving the high-side transistors of said H-bridge via a resistor;

15 two voltage dividers keeping the reference voltage of said high-side drivers on the voltage levels of the midpoints of said H-bridge;

two low-side drivers having an input and an output, wherein the input are control signals from said control logic circuit and a voltage from said power management module and the output is driving the low-side transistors of said H-bridge;

20

two high-side transistors of said H-bridge being connected between battery voltage and the midpoints of said H-bridge having their gates connected to said related high-side drivers;

25 two low-side transistors of said H-bridge being connected between the
mid-points of said H-bridge and ground having their gates connected to said related
high-side drivers; and

a load between the midpoints of said H-bridge.

2. The circuit of claim 1 wherein said control logic, said power management module, the switching part of said means to increase battery voltage, said two high-side drivers, said voltage dividers, and said low-side drivers are all implemented on one ASIC.
3. The circuit of claim 2 wherein said ASIC is built using CMOS technology.
4. The circuit of claim 2 wherein said ASIC is built using DMOS technology.
5. The circuit of claim 2 wherein said ASIC is built using bipolar technology.
6. The circuit of claim 1 wherein said reverse supply protection and said high-side and low-side transistors are implemented outside of an ASIC.
7. The circuit of claim 1 wherein said means to drive at the battery voltage level is a charge pump.
8. The circuit of claim 7 wherein said charge pump comprises a switching network controlled by a clocking scheme.
9. The circuit of claim 8 wherein said clocking scheme is a two-phase clocking scheme.

10. The circuit of claim 7 wherein said charge pump comprises two external capacitors.
11. The circuit of claim 10 wherein said two external capacitors are ceramic capacitors.
12. The circuit of claim 1 wherein said means for external supply protection is driving a transistor to inhibit any reverse supply situation.
13. The circuit of claim 12 wherein said transistor is a N-channel MOS power transistor.
14. The circuit of claim 1 wherein said two high-side transistors are N-channel MOS power transistors.
15. The circuit of claim 1 wherein said two low-side transistors are N-channel MOS power transistors.
16. The circuit of claim 1 wherein the load of said H-bridge is controlled by signals using pulse width modulation (PWM).
17. The circuit of claim 1 wherein said load between the midpoints of said H-bridge is a DC-motor.
18. The circuit of claim 17 wherein the direction of the rotation of said DC-motor is controlled by a direction bit.

19. The circuit of claim 17 wherein the velocity of said DC motor is controlled by signals using pulse width modulation (PWM).

20. The circuit of claim 1 wherein said control logic comprises a digital finite state machine.

21. The circuit of claim 1 wherein said power management module comprises several voltage regulators.

22. The circuit of claim 1 wherein said high-side drivers and said low said drivers work in a push-pull configuration.

23. The circuit of claim 1 wherein each of said high-drivers comprises:

a semiconductor switch;

an analog controller having an input and an output, wherein the input are pulses defining the cycles of said semiconductor switch and the output are currents to control said switch; and

a means to provide a bias voltage to said semiconductor switch.

24. The circuit of claim 23 wherein said semiconductor switch is a CMOS FET.

25. The circuit of claim 23 wherein said means to provide a bias voltage is a resistor.

26. A circuit to drive a high-voltage H-bridge using CMOS technology comprising:

5 a control logic circuit, comprising a digital finite state machine, having an input and an output, wherein the input comprises control signals defining the behavior of said H-bridge and the output are control signals for the high-side and low-side drivers of said H-bridge;

a power management module, comprising several voltage regulators, having an input and an output wherein the input is a battery voltage and the output is a voltage to feed the low-side drivers and means to drive at the battery voltage level;

10 a charge pump to drive the high-side drivers of the H-bridge and a means for reverse supply protection comprising two external capacitors and a switching network controlled by a clocking scheme;

a means for reverse supply protection driving a transistor to inhibit any reverse supply situation;

15 two high-side drivers having an input and an output, wherein the input are control signals from said control logic circuit and a voltage from said charge pump and the output is driving the high-side transistors of said H-bridge via a resistor;

two voltage dividers keeping the reference voltage of said high-side drivers on the voltage levels of the midpoints of said H-bridge;

20 two low-side drivers having an input and an output, wherein the input are control signals from said control logic circuit and a voltage from said power management module and the output is driving the low-side transistors of said H-bridge;

two high-side transistors of said H-bridge being connected between
25 battery voltage and the midpoints of said H-bridge having their gates connected to
said related high-side drivers;

two low-side transistors of said H-bridge being connected between the
mid-points of said H-bridge and ground having their gates connected to said related
high-side drivers; and

30 a load between the midpoints of said H-bridge.

27. The circuit of claim **26** wherein said control logic, said power management module,
the switching part of said charge pump, said two high-side drivers, said voltage
dividers, and said low-side drivers are all implemented on one ASIC.

28. The circuit of claim **27** wherein said ASIC is built using CMOS technology.

29. The circuit of claim **27** wherein said ASIC is built using DMOS technology.

30. The circuit of claim **27** wherein said ASIC is built using bipolar technology.

31. The circuit of claim **26** wherein said reverse supply protection and said high-side and
low-side transistors are implemented outside of an ASIC.

32. The circuit of claim **26** wherein said clocking scheme controlling said charge pump is
a two-phase clocking scheme.

- 33.** The circuit of claim **26** wherein said two external capacitors are ceramic capacitors.
- 34.** The circuit of claim **26** wherein said transistor, being driven by said means for external supply protection, is a N-channel MOS power transistor.
- 35.** The circuit of claim **26** wherein said two high-side transistors are N-channel MOS power transistors.
- 36.** The circuit of claim **26** wherein said two low-side transistors are N-channel MOS power transistors.
- 37.** The circuit of claim **26** wherein the load of said H-bridge is controlled by signals using pulse width modulation (PWM).
- 38.** The circuit of claim **26** wherein said load between the midpoints of said H-bridge is a DC-motor.
- 39.** The circuit of claim **38** wherein the direction of the rotation of said DC-motor is controlled by a direction bit.
- 40.** The circuit of claim **38** wherein the velocity of said DC motor is controlled by signals using pulse width modulation (PWM).

41. The circuit of claim **26** wherein said high-side drivers and said low said drivers work in a push-pull configuration.

42. The circuit of claim **26** wherein each of said high-drivers comprises:

a semiconductor switch;

an analog controller having an input and an output, wherein the input are pulses defining the cycles of said semiconductor switch and the output are currents to control said switch; and

a means to provide a bias voltage to said semiconductor switch.

43. The circuit of claim **42** wherein said semiconductor switch is a CMOS FET.

44. The circuit of claim **42** wherein said means to provide a bias voltage is a resistor.